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| 10/715,073 | 11/17/2003 | Torsten Seidel | P2001,0356 | 3310 |

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| EXAMINER | |
|---|---|
| LE, BRIAN Q | |

| ART UNIT | PAPER NUMBER |
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| 2624 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/715,073 | SEIDEL ET AL. | |
| | Examiner | Art Unit | |
| | BRIAN Q. LE | 2624 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *1-8,15 and 16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**Response to Amendment and Arguments**

1. Applicant's amendment filed October 16, 2008, has been entered and made of record.

2. Applicant's arguments, see Remarks, filed October 16, 2008, with respect to the rejection(s) of claim(s) 9-10 and 13-14 under 35 U.S.C. 102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Ulrich et al. U.S. Pub No. 2003/0039388.

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 9-10 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Maeda et al. U.S. Patent No. 6,947,587 and Ulrich et al. US Pub No. 2003/0039388.

Regarding claim 9, Maeda teaches a method for detecting defects on a semiconductor device within a processing tool (abstract, first 2 lines), the processing tool (FIG. 7) including a device transfer area (a stage which wafer can be placed on) (column 4, line 65 to column 5, line 2), an optical sensor (optically pickup) (column 3, lines 1-5), and an illumination system (column 5, lines 1-3) for illuminating an area monitored by the optical sensor (the light is control by object lens) (column 5, lines 1-13), the method which comprises:

Providing the semiconductor device to the device transfer area (a stage/area with moving capability to pickup semiconductor wafer/device to put it in the transfer stages of processing) (column 4, line 65 to column 5, line 2 and column 21, lines 37- 44);

Recording a first image of the semiconductor device using the optical sensor (optically pick up first image signal) (column 3, line 1);

Transferring the semiconductor device to the processing tool (the process where the stage moves the semiconductor wafer to various stages within the processing tool) (column 5, line 60 to column 6, line 10);

Performing a process step on the semiconductor device (process steps such as scan and alignment) (column 5, lines 18-30 and line 63 to column 6, line 15);

Transferring the semiconductor device back to the device transfer area (the repeat of inspection may be employed again through the stages of processing) (column 21, lines 36-44);

Recording a second image of the semiconductor device using the optical sensor (optically pick up second pattern of image signal) (column 3, lines 2-5);

Comparing the first image with the second image (column 3, lines 4-6); and

issuing a signal in response to the comparison (display detect result after comparison) (column 3, lines 15-18).

Maeda does not explicitly teach a method comprises input slot; output slot; load port for loading semiconductor device adjacent to processing tool; transferring the semiconductor device from the device transfer area to the processing tool via the input slot; recording image of semiconductor device within the processing tool by using the optical sensor; and transfer the semiconductor device vi the output slot.

Ulrich further teaches an inspection method (abstract, first line) comprises input slot (input tray) (page 14, column 1, [0164]); output slot (output tray) (page 14, column 2, [0167]); load port for loading semiconductor device adjacent to processing tool (surface of device and conveyor belt) (page 7, column 2, [0093] and FIG. 3, element 99); transferring the semiconductor device from the device transfer area to the processing tool via the input slot (page 14, column 1, [0164]); recording image of semiconductor device within the processing tool by using the optical sensor (page 4, column 2, [0068]); and transfer the semiconductor device vi the output slot (page 14, column 2, [0167]). Modifying Maeda's method of inspection according to Ulrich would be able to include a machine structures with slots, loading ports and image capturing devices within a system to conveniently transfer inspection materials (page 4, column 2, [0066]). This would improve processing and therefore, it would have been obvious to one of the ordinary skill in the art to modify Maeda according to Ulrich.

Referring to claim 10, Maeda teaches the method wherein the comparing step comprises:

Subtracting one of the images from the other one of the images to generate a subtracted image (find the difference between two images) (column 6, lines 16-26 and column 13, lines 65-67);

Identifying a pattern in the subtracted image (identify a shift or gradation pattern) (column 6, lines 20-25); and

Comparing the pattern with at least one reference pattern (column 13, lines 44-47).

For claim 13, Maeda also teaches the method which comprising recording the first and second images by scanning the semiconductor device during a movement of the semiconductor device across the device transfer area (the processing of moving semiconductor device, take

input image signal and convert it into digital image signal) (column 6, lines 4-15 and column 12, lines 60-67).

Regarding claim 14, Maeda discloses the method which comprises stopping a processing of the inspected semiconductor device in response to the signal (the processing of inspected semiconductor device is within boundary of parameters such as position parameters and thus will be controlled or stopped in response to the signal) (column 8, lines 1-15 and column 14, line 15 to column 15, line 5).

3. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Maeda et al. U.S. Patent No. 6,947,587 and Ulrich et al. US Pub No. 2003/0039388 as applied to claim 9 above, and further in view of Takeuchi et al. U.S. Pub. No. 2002/0093656.

Regarding claim 11, Maeda does not explicitly teach wherein a reference pattern represents a defect on a semiconductor device. Takeuchi teaches an inspection system (abstract) wherein a reference pattern represents a defect on a semiconductor device (page 11, [0181]). Modifying Maeda's method of inspection according to Takeuchi would be able to provide reference image which represents defect. This would improve processing because it helps improve pattern formation for detection (page 2, column 1, first 4 lines) and therefore, it would have been obvious to one of the ordinary skill in the art to modify Maeda according to Takeuchi.

4. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Maeda et al. U.S. Patent No. 6,947,587 and Ulrich et al. US Pub No. 2003/0039388 as applied to claim 9 above, and further in view of Spindt et al. U.S. 6,338,662.

For claim 12, Maeda does not explicitly teach a method wherein the defect is at least one of a particle on a device backside causing a focus spot;

Spindt further teaches an inspection system (column 15, lines 56-65) wherein the defect is a particle (expose remainder of actinic material) (column 12, lines 1-13) on a device backside (column 12, line 14) causing a focus spot (focus openings) (column 12, lines 10-17). Modifying Maeda's method of inspection according to Spindt would be able to comprise a defect wherein a particle on a device backside causing a focus spot. This would improve processing because it helps remedy this defect type (provide lateral spacing and self-alignment) (column 2, lines 15-35) and therefore, it would have been obvious to one of the ordinary skill in the art to modify Maeda according to Spindt.

## *Conclusion*

1. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Contact Information***

1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRIAN Q. LE whose telephone number is (571)272-7424. The examiner can normally be reached on 8:30 A.M - 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Werner can be reached on 571-272-7401. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brian Q Le/
Primary Examiner, Art Unit 2624
Tuesday, February 03, 2009